



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(Case No. 219.003-US)

In the Application of: Yamada

Serial No: 09/865,528

Filed: May 29, 2001

Title: Semiconductor Device Test Method and

**Semiconductor Device Tester** 

**Commissioner for Patents** 

P.O. Box 1450

Alexandria, VA 22313-1450

) Group Art Unit: 2829

Before Examiner: V. Nguyen

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 28, 2004

(person signing this certificate)

Signature

## **SUBMISSION OF ENGLISH TRANSLATIONS**

Dear Sir:

Attached hereto is an English translation of each of the following Japanese patent applications: JP50-63990, JP57-6310, JP62-19707, which were submitted in an Information Disclosure Statement dated March 17, 2004.

Respectfully submitted,

Date: May 28, 2004

Neil A. Steinberg Reg. No. 34,735 650-968-8079